

PROCESSORS HAVING COMPRESSED INSTRUCTIONS AND
METHODS OF COMPRESSING INSTRUCTIONS FOR PROCESSORS

[ABSTRACT OF THE DISCLOSURE]

5 Instructions of a program are stored in compressed
form in a program memory (12). In a processor which
executes the instructions, a program counter (50)
identifies a position in the program memory. An
instruction cache (40) has cache blocks, each for
10 storing one or more instructions of the program in
decompressed form. A cache loading unit (42) includes
a decompression section (44) and performs a cache
loading operation in which one or more compressed-form
instructions are read from the position in the program
15 memory identified by the program counter and are
decompressed and stored in one of the said cache blocks
of the instruction cache. A cache pointer (52)
identifies a position in the instruction cache of an
instruction to be fetched for execution. An
20 instruction fetching unit (46) fetches an instruction
to be executed from the position identified by the
cache pointer. When a cache miss occurs because the
instruction to be fetched is not present in the
instruction cache, the cache loading unit performs such
25 a cache loading operation. An updating unit (48)
updates the program counter and cache pointer in
response to the fetching of instructions so as to
ensure that the position identified by the said program
counter is maintained consistently at the position in
30 the program memory at which the instruction to be
fetched from the instruction cache is stored in
compressed form.

[Fig. 3]